

TOSHIBA MOS MEMORY PRODUCTS

TC55257P-10/PL-10
TC55257P-12/PL-12

32,768 WORD \times 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

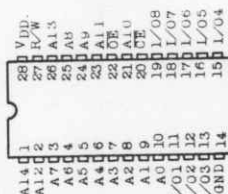
DESCRIPTION

The TC5257P is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and minimum cycle time of 100ns/120ns.

FEATURES

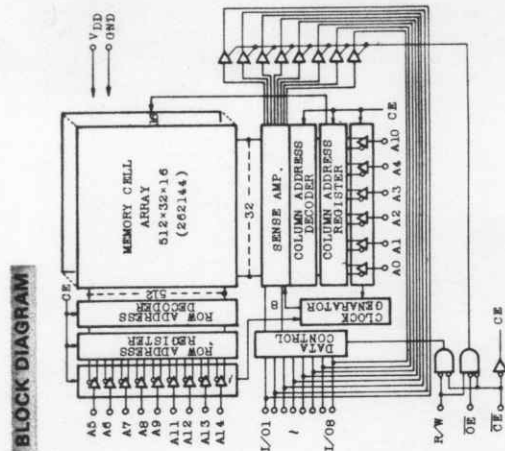
- Low Power Dissipation
27.5mW/MHz(Max.) Operating
Standby Current
- Standby Current
100μA(Max.) : TC55257P-10/PL-12
1mA(Max.) : TC55257P-10/P-12
- 5V Single Power Supply
- Power Down Feature : CE
- Data Retention Supply Voltage : 2.0~5.5V

PIN CONNECTION (TOP VIEW)



PIN NAMES

A ₀ ~A ₁₄	Address Inputs
R/W	Read/Write Control Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{CE}}$	Chip Enable Input
I/O ₁ ~I/O ₈	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground



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Note:

1. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$ or $CE_2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of CE_1 is 2.2V in operation, I_{DD1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In $\overline{CE_2}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_1 \leq 0.2V$.

DEVICE INFORMATION

The TC5C565APL/AFL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1 μF decoupling capacitor for every device is recommended to eliminate such noise.

• DIP 28 PIN OUTLINE DRAWING (6D28A-P)

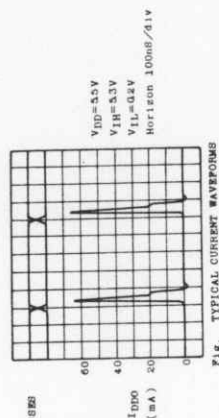
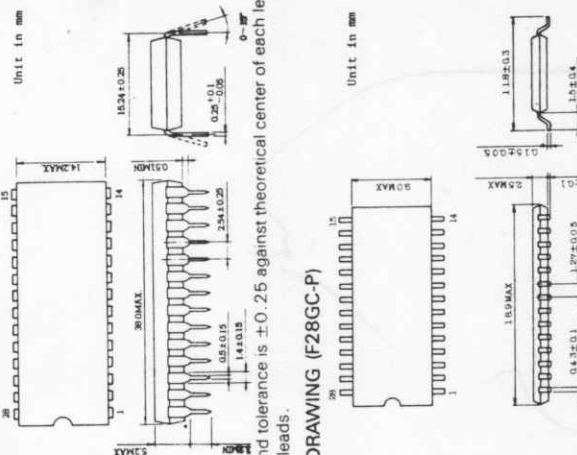


Fig. 1. TYPICAL CURRENT WAVEFORMS



Note : Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

• MFP 28 PIN OUTLINE DRAWING (F28GC-P)

Note : Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described: no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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OPERATION MODE

OPERATION MODE	CE	OE	R/W	I/O, -I/O _s	POWER
Read	L	L	H	Dout	I _{DD}
Write	L	*	L	Din	I _{DD}
Output Deselect	L	H	H	High-Z	I _{DD}
Standby	H	*	*	High-Z	I _{DD}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-0.3~7.0	V
V _{IO}	Input and Output Voltage	-0.5~V _{DD} +0.5	V
P _D	Power Dissipation	1.0	W
T _{SDR}	Soldering Temperature	260~10	°C-sec
T _{STG}	Storage Temperature	-55~150	°C
T _{OPR}	Operating Temperature	0~70	°C

* : -0.3V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IN}	Input High Voltage	2.2	—	V _{DD} +0.3	V
V _L	Input Low Voltage	-0.3*	—	0.8	V
V _{OH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : -0.3V at Pulse width 50ns

D. C. and OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} =0~V _{DD}	—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} =2.4V	-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} =0.4V	4.0	—	—	mA
I _{LO}	Output Leakage Current	CE = V _{IN} or R/W = V _L or OE = V _{IN} V _{DD} =0~V _{DD}	—	—	±1.0	μA
I _{DD1}	Operating Current (Read Cycle)*	V _{DD} =5.5V CE = V _L , R/W = V _{IN} Other Input = V _{IN} /V _L I _{OUT} =0mA	t _{cycle} =1μs	—	10	mA
I _{DD2}		V _{DD} =5.5V CE = 0.2V R/W = V _{DD} -0.2V Other Input = V _{DD} -0.2V/0.2V I _{OUT} =0mA	t _{cycle} =1μs	—	45	mA
I _{DD1}		CE = V _{IN}	—	—	5	mA
I _{DD2}		CE = V _{DD} -0.2V V _{DD} =2.0~5.5V	—	—	40	mA
I _{DD1}	Standby Current	CE = V _{IN}	—	—	3	mA
I _{DD2}	Standby Current	CE = V _{DD} -0.2V V _{DD} =2.0~5.5V	—	—	100	μA

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle.

CAPACITANCE

(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} =GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

(Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257P-10 MIN. MAX.	TC55257P-12 MIN. MAX.	UNIT
t _{RC}	Read Cycle Time	V _{IN} =2.4V/0.6V	100	120	—
t _{ACC}	Address Access Time	V _{IN} =2.2V	—	100	120
t _{CO}	CE Access Time	V _L =0.8V	—	100	120
t _{OE}	Output Enable to Output in Valid	t _r , t _f ≤5ns	—	50	60
t _{OE}	Chip Enable(CE) to Output in Low-Z	V _{OH} =2.2V	10	10	ns
t _{OE}	Output Enable to Output Low-Z	V _{OL} =0.8V	5	5	—
t _{OD}	Chip Enable (CE) to Output in High-Z	Output Load : C _L (100pF)and 1 TTL Gate	—	50	60
t _{OD}	Output Enable to Output in High-Z	—	—	40	50
t _{OH}	Output Data Hold Time	—	10	10	—

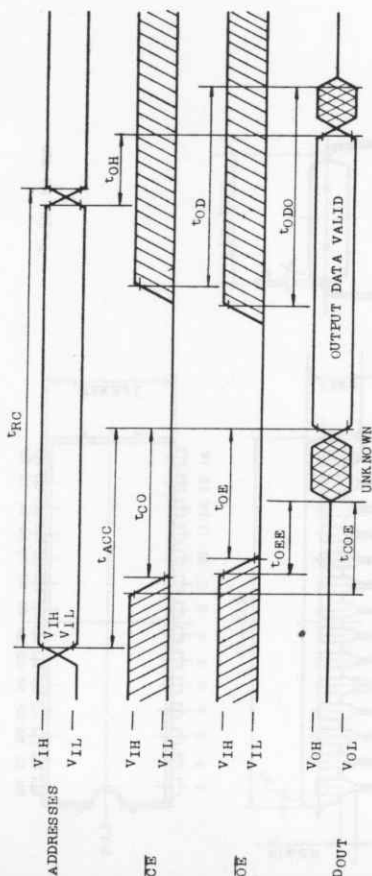
Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257P-10 MIN. MAX.	TC55257P-12 MIN. MAX.	UNIT
t _{WC}	Write Cycle Time	V _{IN} =2.4V/0.6V	100	120	—
t _{WP}	Write Pulse Width	V _{IN} =2.2V	70	80	—
t _{OW}	Chip Selection to End of Write	V _L =0.8V	90	100	—
t _{AS}	Address Set up Time	t _r , t _f ≤5ns	0	0	—
t _{WR}	Write Recovery Time	—	10	10	—
t _{OW}	R/W to Output High-Z	—	50	60	ns
t _{OW}	R/W to Output Low-Z	—	10	10	—
t _{OS}	Data Set Up Time	—	40	50	—
t _{OH}	Data Hold Time	—	0	0	—

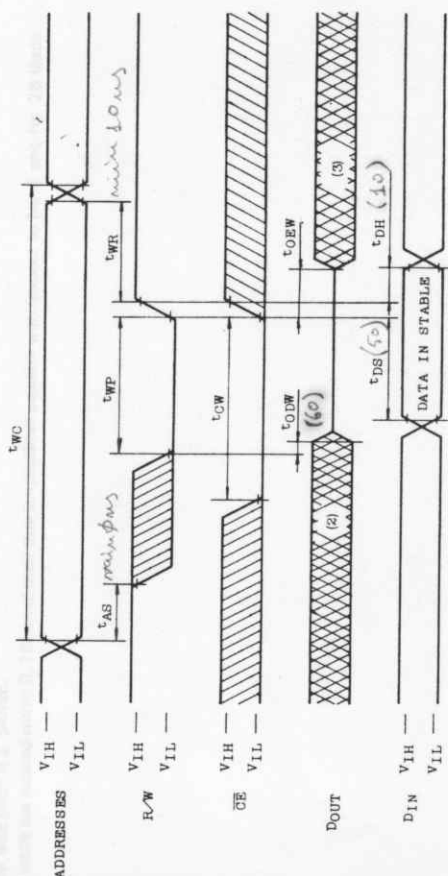
Note : Input pulse levels = V_{IN}
Timing Measurement Reference levels = V_{IN}, V_L

TIMING WAVEFORMS

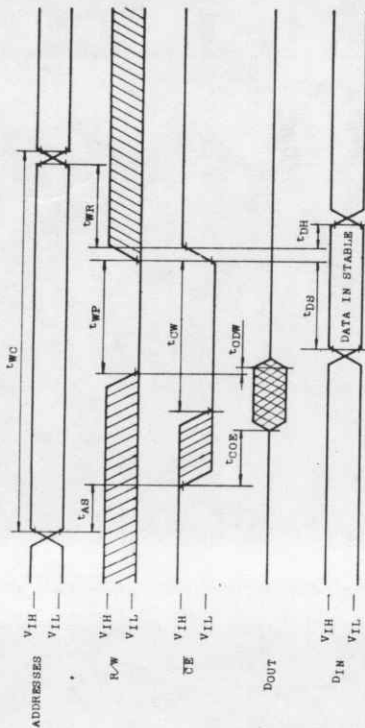
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



• WRITE CYCLE 2 (4) (CE Controlled Write)



Note: 1. R/W is High for Read cycle.

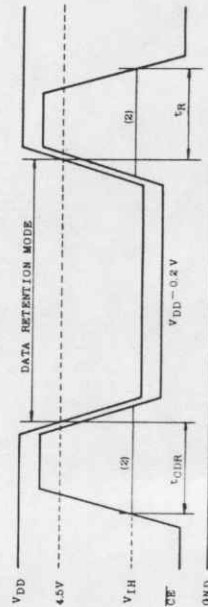
- Assuming that CE low transition occurs coincident with or after R/W Low transition. Outputs remain in a high impedance state.
- Assuming that CE High transition occurs coincident with or prior to R/W High transition. Outputs remain in a high impedance state.
- Assuming that OE is High for Write Cycle. Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DSZ}	Standby Supply Current	—	—	50	μA
t_{DNR}	Chip Deselection to Data Retention Mode Recovery Time	—	—	1.0	ms
t_R	Read cycle time	0	—	—	ns

Note (1): Read cycle time.

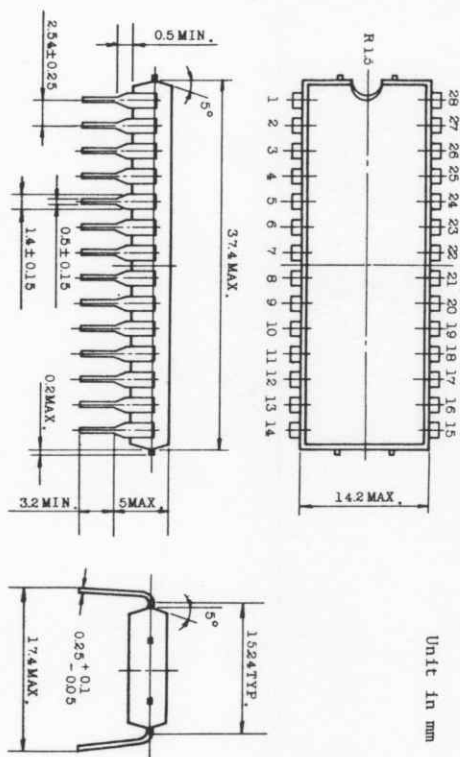
CE Controlled Data Retention Mode



Note (2): If the V_{DH} of CE is 2.4V in operation, I_{DSZ} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

TC55257P-10/PL-10
TC55257P-12/PL-12

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

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